

Seamless Integration of Photonic Circuit Simulation and Layout Design



Introduction

VPIphotonics and Luceda Photonics streamline the design process for Photonic Integrated Circuits. For this purpose, our design flows support a set of common foundry-validated Process Design Kits (PDKs). Designers can benefit from a flow that starts from a graphical photonic integrated circuit design and system simulation environment which seamlessly couples to Python scripted layout and design capabilities for tape-out.

Luceda's *IPKISS Design Platform* combines circuit level design and simulation, layout and device CAD all based on Python scripting. Luceda allows

designers to tape out to the foundries by means of foundry validated PDKs.

VPIcomponentMaker Photonic Circuits is a professional simulation and design environment for large-scale photonic integrated circuits, which offers a mix of general-purpose photonic, electrical and optoelectronic device models.

The dedicated extensions *VPItoolkitPDK <fab>* enable a layout-aware schematic-driven PIC design workflow and provide access to a broad set of available standard building blocks (BBs) of the specific foundry PDK.

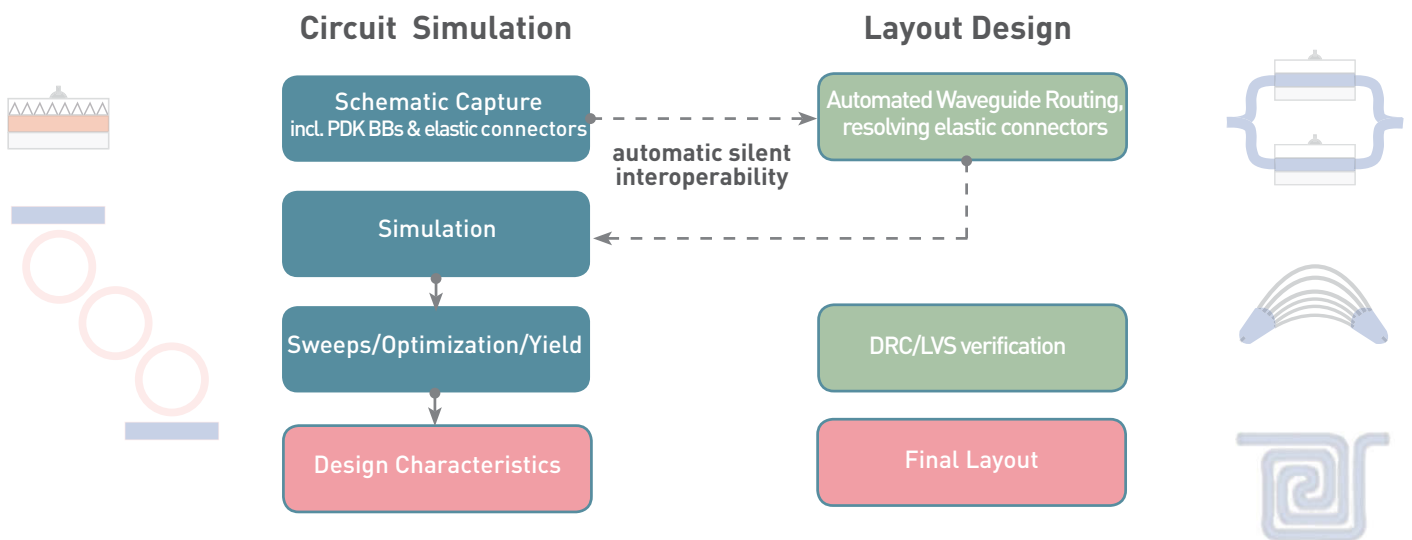


Figure 1 Sketch of layout-aware schematic-driven design methodology



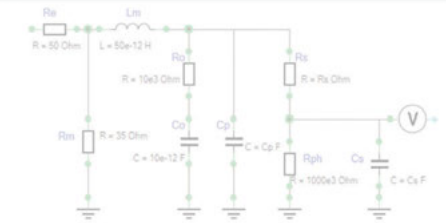
Features and Benefits



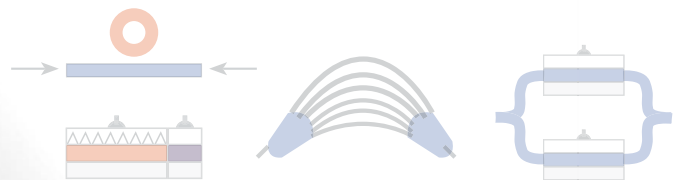
- ✓ Use *VPIcomponentMaker Photonic Circuits* and *VPItoolkit PDK <fab>* extensions to design and simulate the PIC within a complete optical or opto-electrical system employing a library of active and passive PDK BBs with realistic foundry-specific simulation models.
- ✓ Seamlessly generate the Python based layout of your circuit within the *IPKISS Design Platform* using the foundry PDK and improve the yield and reliability of your PIC design flow.
- ✓ Combine graphical schematic capture and automated waveguide routing employing the layout-aware schematic-driven PIC design methodology [1, 2]. This approach is delivered by:
 - seamless integration of circuit and layout tools via smart elastic optical connectors
 - capability to specify exact physical locations and orientations of PDK BBs on the final layout while performing graphical schematic capture.

A circuit simulator invokes a layout design tool (automatically and invisibly for users) to determine the actual physical lengths and shapes of automatically routed elastic connectors, constructs compact simulation models for them, and after that initiates the circuit simulations as schematically described in Figure 1.

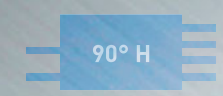
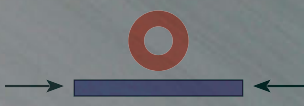
Refer to the application example in Figure 2 to see how the port locations are specified and the elastic connectors are used on the schematic. Note that absolute, relative, and parameterized locations are supported.



- ✓ Sweep and optimize the values of one or more schematic parameters, including the parameters which affect the circuit layout, for achieving a desired circuit behavior.
- ✓ Extend the list of PDK BBs with your own custom components not covered by the list of foundry-certified PDK BBs. Importantly, all such custom PDK BBs will support the layout-aware schematic-driven design capabilities and the export of their layout to Luceda's *IPKISS Design Platform* (Figure 3).
- ✓ Leverage support of multilevel hierarchical designs and reuse your subcircuits as compound BBs in other designs, thus conveniently handling design complexity of large-scale PICs.
- ✓ Quickly generate a GDS mask of the designed circuit directly from your circuit schematic view in *VPIcomponentMaker Photonic Circuits* via *IPKISS* called in the background. The GDS mask can be additionally opened and shown by other tools such as *KLayout* for immediate verification.
- ✓ Investigate and validate your PIC functionality in system application of interest employing seamless interface with *VPItransmissionMaker Optical Systems*.



Please refer to the design examples in Figures 2 and 3, for which schematic representation in *VPIphotonics Design Suite*, the corresponding layout in Luceda's *IPKISS Design Platform*, and the simulation results are shown.



Design Examples Using PDK Libraries

Widely Tunable Laser

Figure 2 shows a design example of a widely tunable laser based on the PDK for an InP-based PIC foundry process by SMART Photonics [3]. Both *VPIcomponentMaker* and *IPKISS* provide PDKs for this process.

Figure 2 a) Simulation schematic created in *VPIcomponentMaker* Photonic Circuits using BBs of *VPItoolkit* PDK SMART, including elastic connectors, and examples of port locations

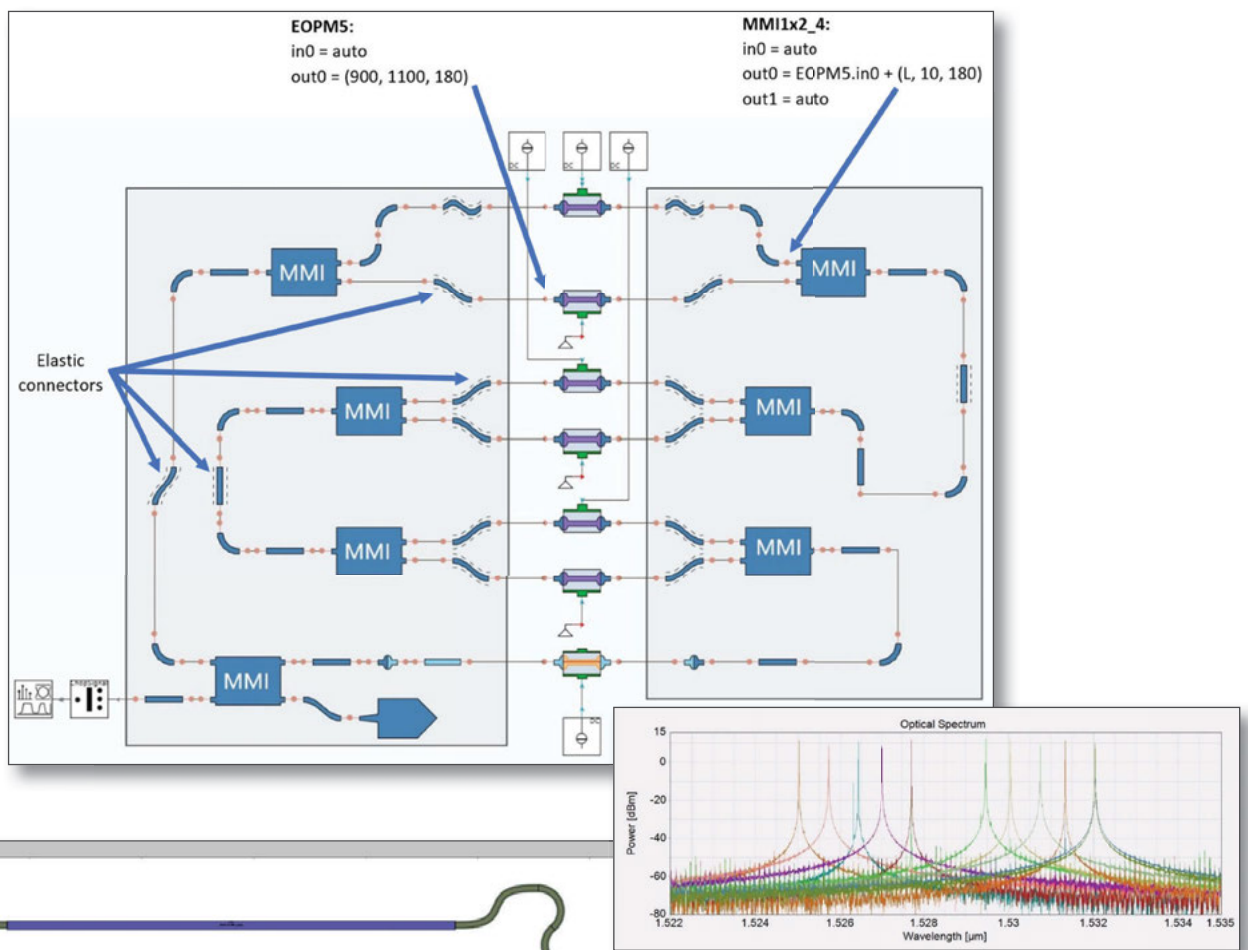
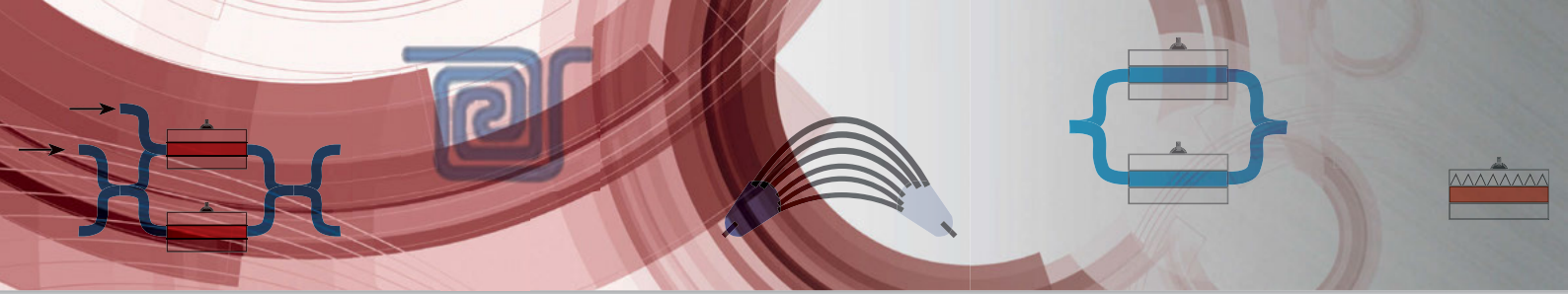


Figure 2 b) Exemplary simulation results demonstrating the laser tuning characteristics

Figure 2 c) The corresponding automatically exported mask layout in *Luceda's IPKISS Design Platform*





Integrated Optical Buffer

Figure 3 shows a design example of an integrated optical buffer based on the PDK for a SiN-based PIC foundry process by LIGENITEC [4]. Both *VPIcomponentMaker* and *IPKISS* provide PDKs for this process.

Figure 3 a) Simulation schematic created in *VPIcomponentMaker Photonic Circuits* using BBs of *VPItoolkit PDK LIGENITEC*, including elastic connectors, and a custom component for waveguide delay line

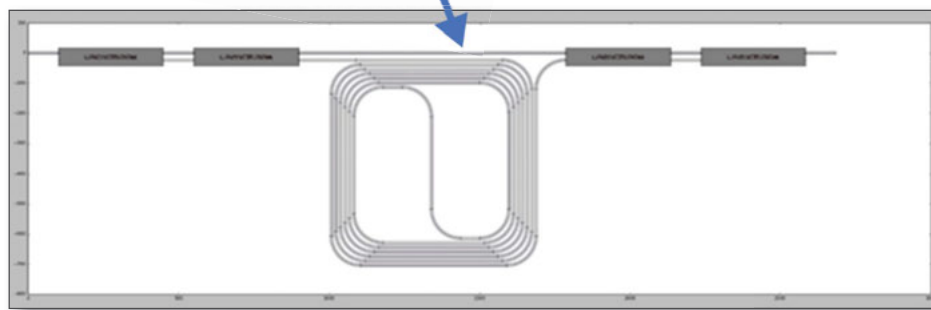
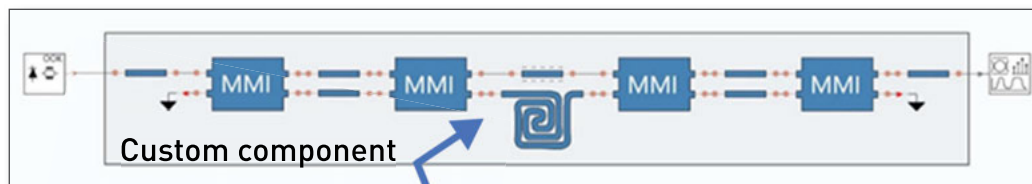


Figure 3 b) The corresponding automatically exported mask layout in Luceda's *IPKISS Design Platform*

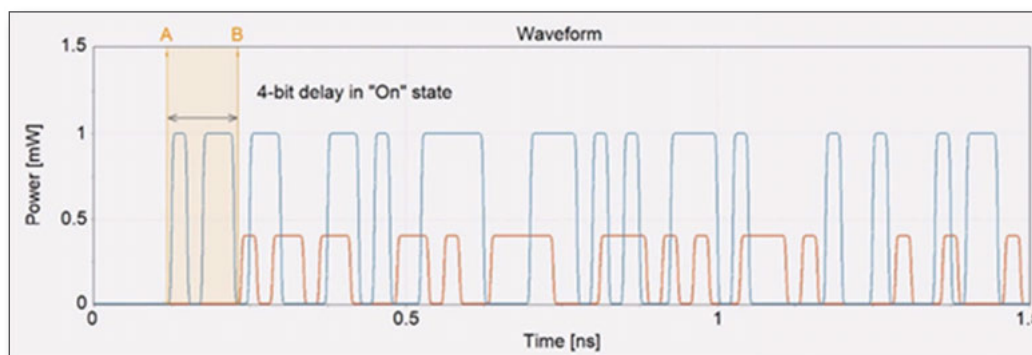


Figure 3 c) Exemplary simulation results of a 4-bit delay for the output signal introduced by the optical buffer in "switched-on" state

References

1. S. F. Mingaleev, S. G. Savitski, E. S. Sokolov, I. G. Koltchanov, and A. Richter, Layout-Aware Schematic-Driven Design Methodology for Photonic Integrated Circuits, European Conference on Integrated Optics, p-21 (2016).
2. S. Mingaleev, A. Richter, E. Sokolov, S. Savitzki, A. Polatynski, J. Farina, and I. Koltchanov, Rapid virtual prototyping of complex photonic integrated circuits using layout-aware schematic-driven design methodology, Proc. SPIE 10107, art. 1010708 - 15 pages (2017).
3. SMART Photonics, <https://smartphotonics.nl> [accessed 28 July 2020].
4. LIGENITEC, <https://www.ligentec.com> [accessed 28 July 2020].

